CLAIMS

1. A method for manufacturing buried connections in an integrated circuit, comprising:

providing a structure formed of a first support wafer glued onto a rear surface of a thin semiconductor wafer, one or several elements of the integrated circuit being possibly formed in and above the thin wafer;

gluing a second support wafer on the structure on the front surface side of the thin wafer;

removing the first support wafer;

forming connections between different areas of the rear surface of the thin wafer;

gluing a third support wafer on the connections; and

removing the second support wafer.

2. The method of claim 1, wherein the thin wafer and the first support wafer are glued via an insulating wafer.

3. The method of claim 1, wherein the step of forming the connections comprises the steps of:

etching openings in an insulating layer formed on the rear surface of the thin wafer; and

filling the openings with a conductive material.

4. The method of claim 3, further comprising after the step of etching openings in the insulating layer, a step of etching areas of reduced thickness in the insulating layer, the areas of reduced thickness being then filled like said openings with a conductive material.

5. The method of claim 3, wherein the filling of the openings with a conductive material comprises:

depositing a metal layer on the structure on the side of the insulating layer and of the openings;

annealing to form a silicide layer at the bottom of the openings.

6. The method of claim 3, comprising, after the step of filling the openings and possibly the areas of reduced thickness:

performing a chem-mech polishing of the conductive filling material to expose the insulating layer to obtain a planar surface;

covering said planar surface with a second insulating layer; and

gluing the third support wafer on the second insulating layer.

7. The method of claim 1, comprising, prior to the gluing of the second support wafer, a step of covering the structure with a bonding layer.

8. An integrated circuit comprising components formed in and above a thin semiconductor wafer attached on a support wafer placed at the rear surface of the thin wafer, the rear surface of the thin wafer being covered with a first insulating layer comprising openings cross the thin wafer, the openings containing conductive portions in contact with some areas of the rear surface of the thin semiconductor wafer, said conductive portions being made of silicide.

9. The integrated circuit of claim 8, wherein some of the said conductive portions are in contact with conductive wells crossing the thin wafer, the conductive wells being eventually made of silicide.